

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims 1-25:**

1. – 18. (cancelled)

19. (currently amended) A method for manufacturing a defect-free silicon single crystal in which void defects, OSFs (oxidation induced stacking faults), and dislocation clusters (interstitial silicon dislocation defects) have been eliminated ~~by setting a carbon concentration to  $1 \times 10^{15}$  atoms/cm<sup>3</sup> or less~~ ~~By setting a concentration of  $1 \times 10^{15}$  atoms/cm<sup>3</sup> or less and adjusting a growth condition V/G (V: growth rate, G: axial temperature gradient of the crystal)~~ by setting a carbon concentration to  $1 \times 10^{15}$  atoms/cm<sup>3</sup> or less for suppressing occurrence of the dislocation clusters, thereby expanding an allowable range of a growth condition V/G (V: growth rate, G: axial temperature gradient of a crystal) in which a defect-free crystal can be produced, and adjusting the growth condition V/G within the expanded allowable range.

20. (cancelled)

21. (currently amended) A method for pulling a silicon single crystal using a silicon single crystal pulling apparatus comprising: a single crystal pulling chamber in which a carrier gas is supplied from above and exhausted from below; a quartz crucible that is provided inside the single crystal pulling chamber, and into which a raw material is supplied and melted;

a graphite crucible that covers an outside of the quartz crucible; and a heat shield that is disposed above the quartz crucible and the graphite crucible, for guiding the carrier gas to a melt surface inside the quartz crucible, in which the silicon single crystal is pulled from the melt inside the crucible, the heat shield being arranged to be raised and lowered,

the method comprising:

in a process of melting a polycrystalline silicon, positioning the heat shield  
~~where a carbon concentration inside the pulled silicon single crystal is  $3 \times 10^{15}$~~   
~~atoms/cm<sup>3</sup> or less,~~

at a position where a distance between an upper end of the heat shield and an inner wall of the single crystal pulling chamber is 0-30mm, thereby suppressing flow of CO gas to the melt, the CO gas being generated by a reaction between the quartz crucible and the graphite crucible which passes through the upper end of the heat shield and the inner wall of the single crystal pulling chamber,

setting a carbon concentration to  $1 \times 10^{15}$  atoms /cm<sup>3</sup> or less, thereby expanding and allowable range of growth condition V/G in which a defect-free crystal can be produced,

and pulling up the silicon single crystal while a growth condition V/G (V: growth rate, G: axial temperature gradient of the crystal) is adjusted within the defect-free allowable range such that void defects, OSFs (oxidation induced stacking faults), and dislocation clusters (interstitial silicon dislocation defects) are eliminated from the pulled silicon single crystal.

22. (cancelled)

23. (cancelled)

24. (new) A silicon wafer, acquired by pulling from a silicon melt while maintaining a growth condition V/G (V: growth rate, G: axial temperature gradient of a crystal) within a void defect region,

wherein no OSF (oxidation induced stacking fault) region is present in the silicon wafer, and an average void defect density is not more than  $5 \times 10^6/\text{cm}^3$ , and an average void defect size is not more than 100nm.

25. (new) A silicon wafer, acquired by pulling from a silicon melt while maintaining a growth condition V/G (V: growth rate, G: axial temperature gradient of a crystal) within a void defect region,

wherein no OSF (oxidation induced stacking fault) region is present in a plane of the silicon wafer at least from a center of the plane up to 10mm from an outer periphery, an average void defect density in the silicon wafer from a center axis of the silicon wafer to 10 mm from an other periphery of the silicon wafer is not more than  $5 \times 10^6/\text{cm}^3$ , and an average void defect size is not more than 100nm.